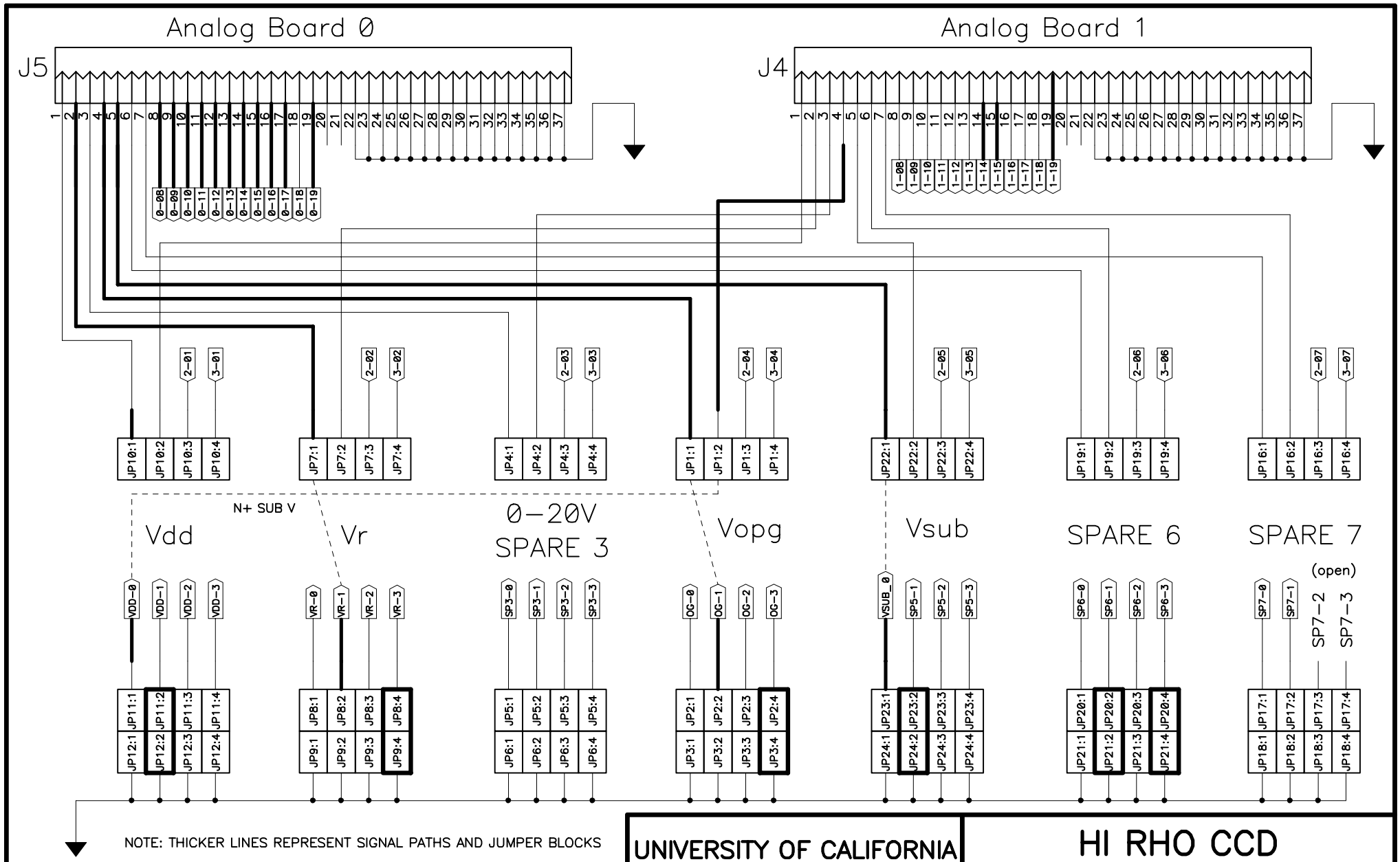

REVISION

09–20–00	MOVED H2AL AND H3AL
09–26–00	CHANGED 'RESET' SIGNAL NAME TO Vrg
06–19–01	MOVED H2AL AND H3AL FROM BOARD 1 PINS 9 AND 10 TO 14 AND 15
07–05–01	ADDED CONNECTIONS FOR BOARDS 0 AND 1 PIN 19 FOR SYNC SIGNALS
07–10–01	ADDED WIRE FROM DCR/SPARE17 PIN TO VDD–0 OUTPUT PIN. THIS ADDS N+ SUB VOLTAGE FROM BOARD0 PIN17 TO OUTPUT PIN A1.
08–07–01	Vopg1 NOW GOES TO Vdd0 OUTPUT

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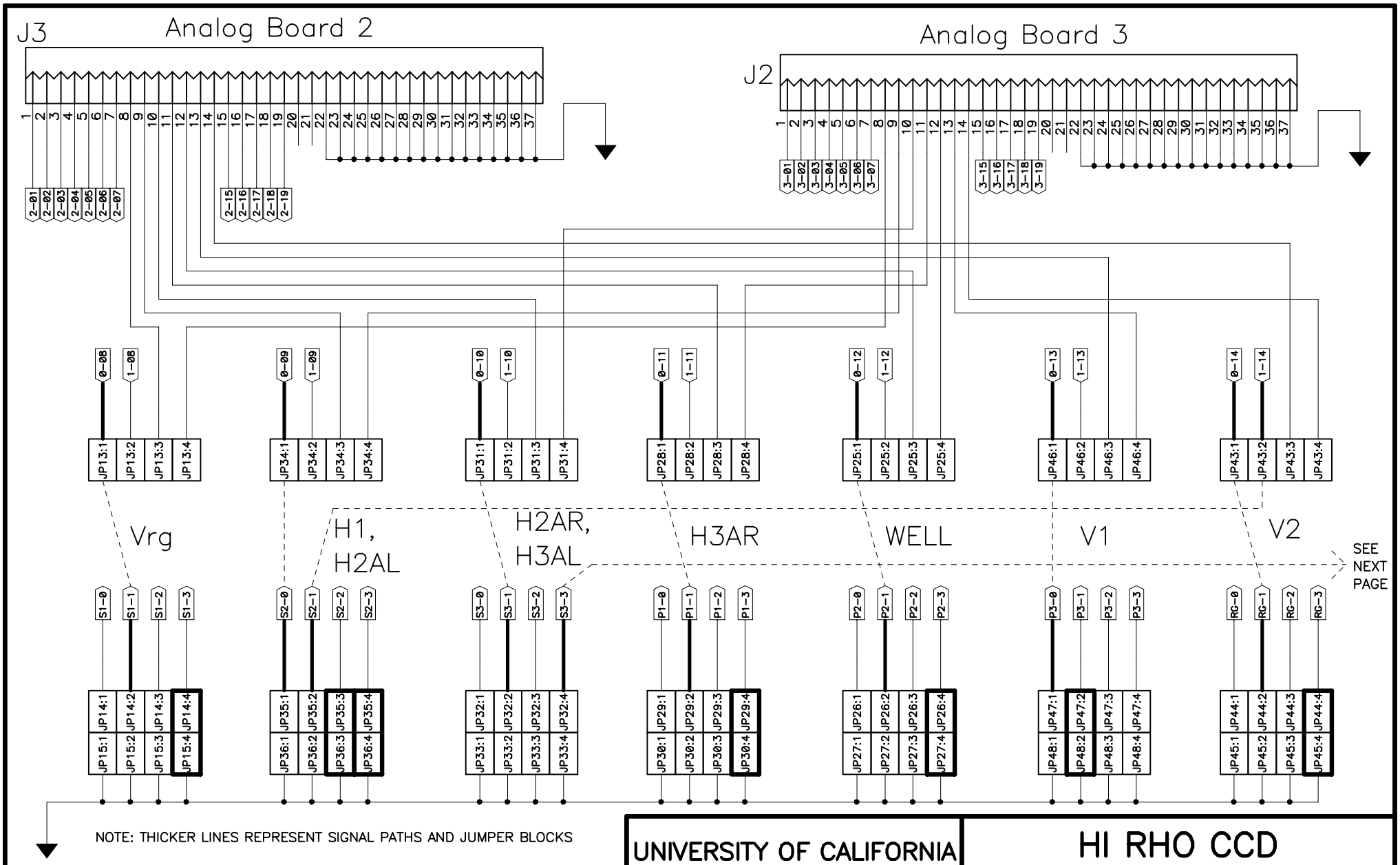
LICK OBSERVATORY

HI RHO CCD INTERCONNECT BOARD

DES'N BY: B. Alcott
ORIGIN DATE: 7–25–96
DRAWN BY:
MODIFY DATE:08–07–01
PATH: HI_RHO_CCD\HI_RHO_INTERCONNECT
REV. B

DWG. NO. EL–1281

NUM. 1 OF 5



NOTE: THICKER LINES REPRESENT SIGNAL PATHS AND JUMPER BLOCKS

REVISION

09-20-00 MOVED H2AL AND H3AL
09-26-00 CHANGED 'RESET' SIGNAL NAME TO Vrg
06-19-01 MOVED H2AL AND H3AL FROM BOARD 1 PINS 9 AND 10 TO 14 AND 15

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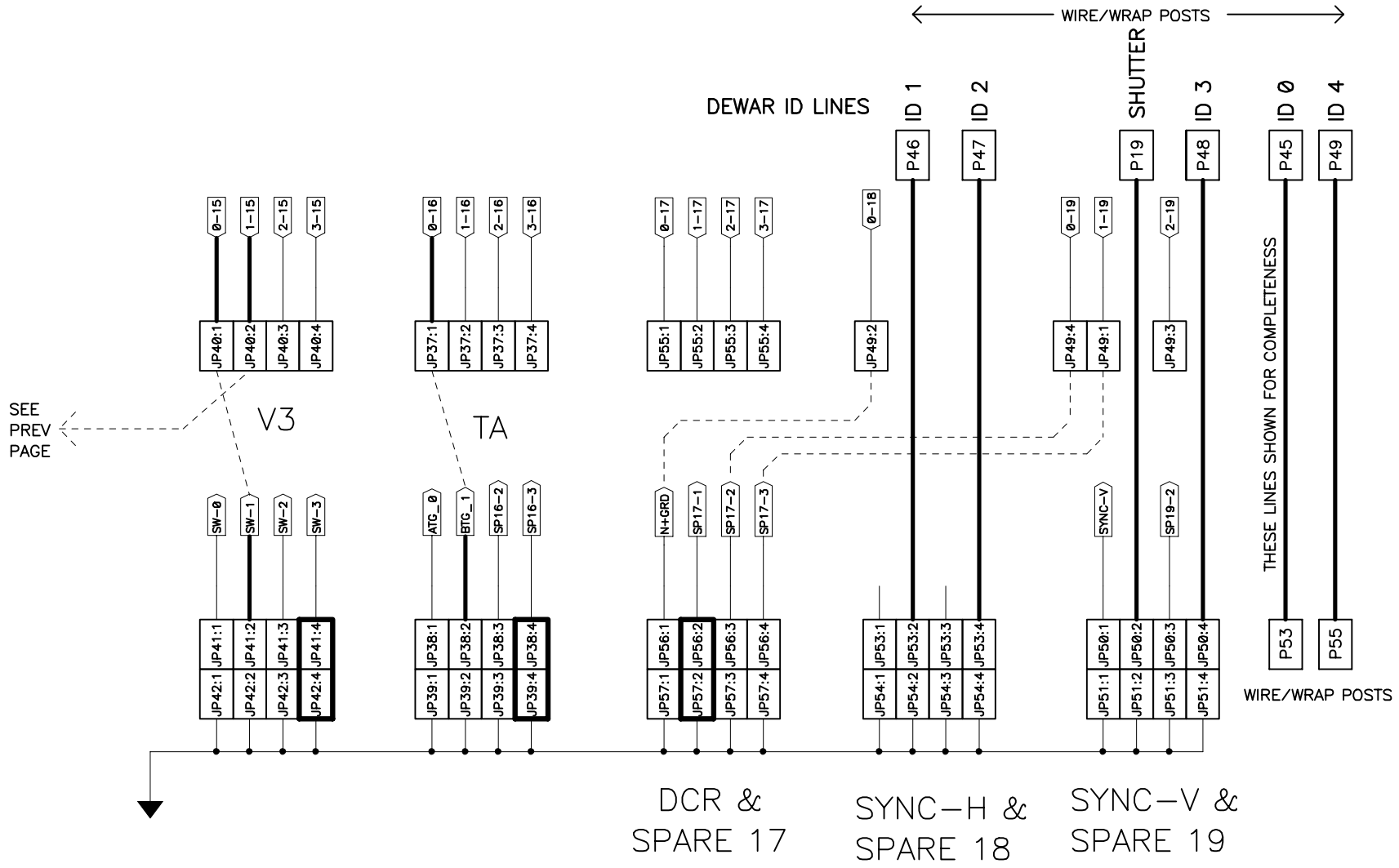
HI RHO CCD INTERCONNECT BOARD

DES'N BY: B. Alcott	ORIGIN DATE: 7-25-96	DWG. NO.	NUM. 2 OF 5
DRAWN BY:	MODIFY DATE:06-19-01	EL-1281	
PATH: HI_RHO_CCD\HI_RHO_INTERCONNECT	REV. B		



NOTE: THICKER LINES REPRESENT SIGNAL PATHS AND JUMPER BLOCKS

REVISION

09–20–00 MOVED H2AL AND H3AL
09–26–00 MOVED DEWAR ID LINES FROM SPARE–17 TO SPARE–18 JUMPER BLOCKS
06–19–01 MOVED H2AL AND H3AL FROM BOARD 1 PINS 9 AND 10 TO 14 AND 15
07–05–01 ADDED CONNECTIONS FOR BOARDS 0 AND 1 PIN 19 FOR SYNC SIGNALS
07–10–01 ADDED WIRE FROM DCR/SPARE17 PIN TO VDD–0 OUTPUT PIN. THIS ADDS N+ SUB VOLTAGE FROM BOARD0 PIN17 TO OUTPUT PIN A1.
08–07–01 REMOVED OUTPUT FROM 0–17

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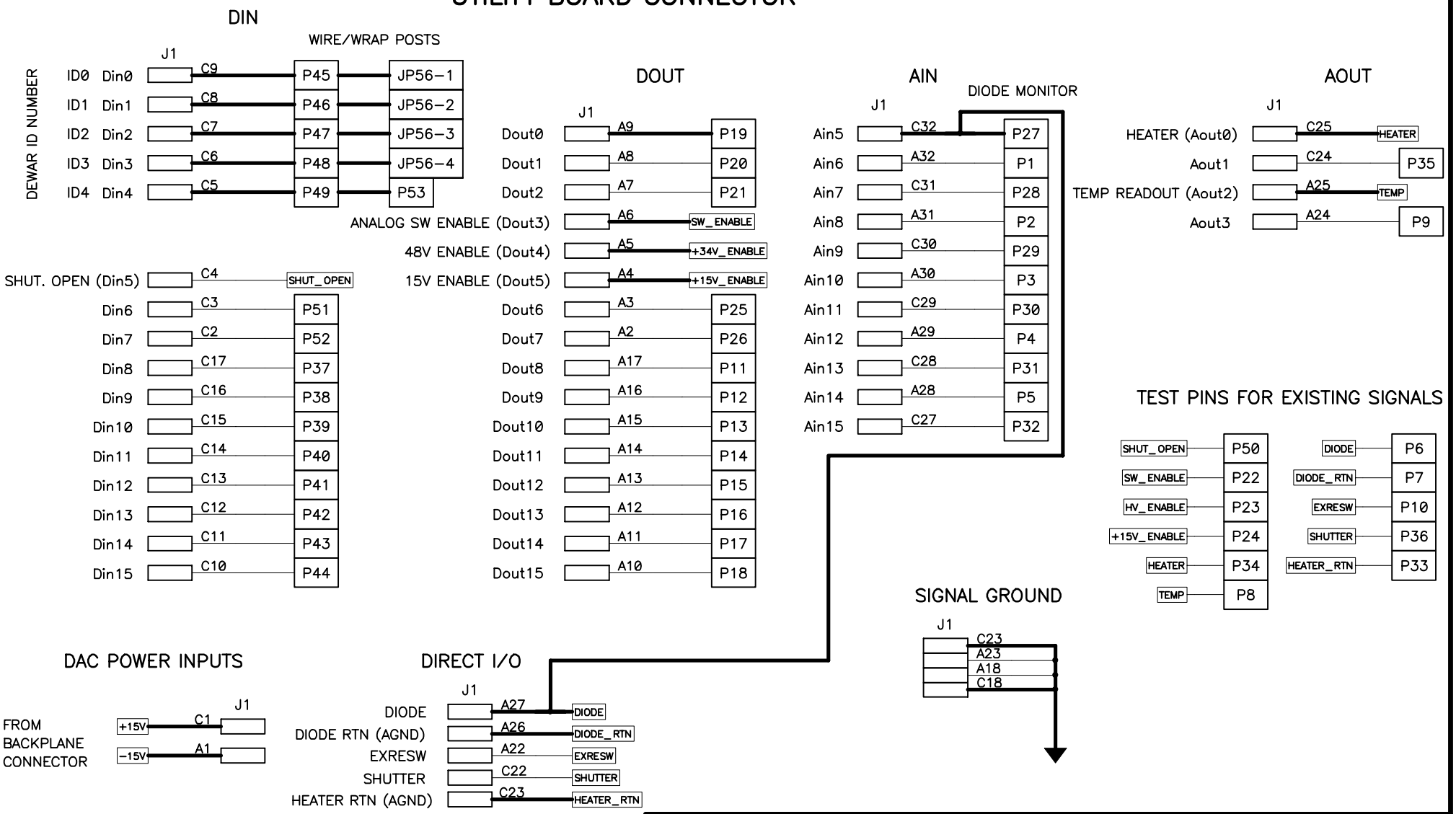
HI RHO CCD INTERCONNECT BOARD

DES'N BY: B. Alcott
ORIGIN DATE: 7–25–96
DRAWN BY:
MODIFY DATE:08–07–01
PATH: HI_RHO_CCD\HI_RHO_INTERCONNECT
REV. B

DWG. NO. EL–1281
NUM. 3 OF 5

UTILITY BOARD CONNECTOR



NOTE: THICKER LINES REPRESENT SIGNAL PATHS

REVISION

09-20-00 MOVED H2AL AND H3AL
06-15-01 CORRECTED VARIOUS PIN NUMBERS AND LABELS
07-05-01 CHANGED REFERENCES FROM 48V TO HV (HIGH VOLTAGE)

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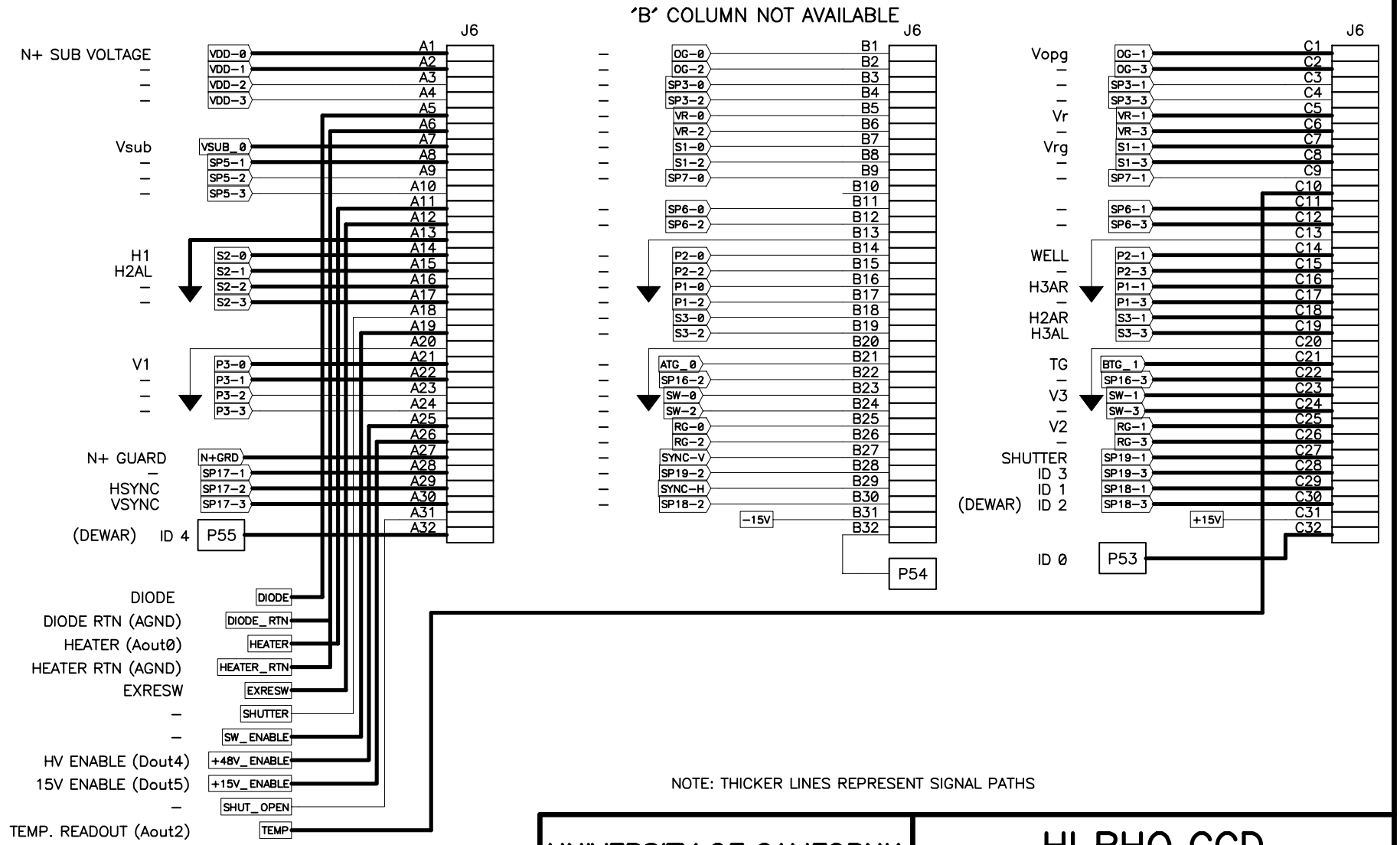
HI RHO CCD INTERCONNECT BOARD

DES'N BY: B. Alcott	ORIGIN DATE: 7-25-96	DWG. NO.	NUM. 4 OF 5
DRAWN BY:	MODIFY DATE: 06-15-01	EL-1281	
PATH: HI_RHO_CCD\HI_RHO_INTERCONNECT	REV. B		

BACKPLANE CONNECTOR



NOTE: THICKER LINES REPRESENT SIGNAL PATHS

REVISION

09-20-00	MOVED H2AL AND H3AL
09-26-00	CHANGED 'RESET' SIGNAL NAME TO Vrg
07-05-01	CHANGED REFERENCES FROM 48V TO HV (HIGH VOLTAGE)
07-05-01	ADDED CONNECTIONS FOR BOARDS 0 AND 1 PIN 19 FOR SYNC SIGNALS
07-10-01	ADDED WIRE FROM DCR/SPARE17 PIN TO VDD-0 OUTPUT PIN. THIS ADDS N+ SUB VOLTAGE FROM BOARD0 PIN17 TO OUTPUT PIN A1.

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HI RHO CCD INTERCONNECT BOARD

DES'N BY: B. Alcott	ORIGIN DATE: 7-25-96	DWG. NO.	NUM. 5 OF 5
DRAWN BY:	MODIFY DATE: 07-10-01	EL-1281	
PATH: HI_RHO_CCD\HI_RHO_INTERCONNECT	REV. B		