HI RHO CCD

CLOCK CABLE #1

37 PIN CONNECTOR

PIN	NAME	FUNCTION	RANGE	CODE	PIN	NAME
1	Vdd	OUTPUT DRAIN (UNUSED)	0 ->+27	FD	20	–
2	Vr	RESET DRAIN (UNUSED)	0->+19	FB	21	–
3	–	---	0->+20	F7	22	GND
4	Vopg	OUTPUT XFR GATE	–5->+5	EF	23	GND
5	Vsub	SUBSTRATE	–10->+10	DF	24	GND
6	–	---	–10->+10	BF	25	GND
7	–	---	–10->+10	7F	26	GND
8	Vrg	RESET GATE	–10->+10CLOCKED	0	27	GND
9	H1	HORIZONTAL PHASE 1	–10->+10CLOCKED	1	28	GND
10	H2AR	HORIZONTAL PHASE 2 (R)	–10->+10CLOCKED	2	29	GND
11	H3AR	HORIZONTAL PHASE 3 (R)	–10->+10CLOCKED	3	30	GND
12	WELL	SUMMING WELL	–10->+10CLOCKED	4	31	GND
13	V1	VERTICAL PHASE 1	–10->+10CLOCKED	5	32	GND
14	V2	VERTICAL PHASE 2	–10->+10CLOCKED	6	33	GND
15	V3	VERTICAL PHASE 3	–10->+10CLOCKED	8	34	GND
16	TA	TRANSFER GATE	–10->+10CLOCKED	8	35	GND
17	N+ SUB V	N+ SUB VOLTAGE	–10->+10CLOCKED	9	36	GND
18	N+ GRD	N+ GUARD CONTROL	–10->+10CLOCKED	A	37	GND
19	HSYNC	HORIZONTAL SYNC	–10->+10CLOCKED	B		

ANALOG CARD #0

CLOCK CABLE #2

37 PIN CONNECTOR

PIN	NAME	FUNCTION	RANGE	CODE	PIN	NAME
1	–	---	0 ->+27	FD	20	–
2	–	---	0->+19	FB	21	–
3	–	---	0->+20	F7	22	GND
4	–	---	–5->+5	EF	23	GND
5	–	---	–10->+10	DF	24	GND
6	–	---	–10->+10	BF	25	GND
7	–	---	–10->+10	7F	26	GND
8	–	---	–10->+10CLOCKED	0	27	GND
9	–	---	–10->+10CLOCKED	1	28	GND
10	–	---	–10->+10CLOCKED	2	29	GND
11	–	---	–10->+10CLOCKED	3	30	GND
12	–	---	–10->+10CLOCKED	4	31	GND
13	–	---	–10->+10CLOCKED	5	32	GND
14	H2AL	HORIZONTAL PHASE 2 (L)	–10->+10CLOCKED	6	33	GND
15	H3AL	HORIZONTAL PHASE 3 (L)	–10->+10CLOCKED	8	34	GND
16	–	---	–10->+10CLOCKED	8	35	GND
17	–	---	–10->+10CLOCKED	9	36	GND
18	–	---	–10->+10CLOCKED	A	37	GND
19	VSYNC	VERTICAL SYNC	–10->+10CLOCKED	B		

ANALOG CARD #1

REVISION

09–20–00 MOVED H2AL AND H3AL FROM PINS 14 AND 15 TO 9 AND 10
09–21–00 ADDED DC RESTORE
06–19–01 MOVED H2AL AND H3AL BACK TO PINS 14 AND 15. REMOVED DC RESTORE AND ADDED N+ GUARD TO PIN 18 OF BOARD 0
06–20–01 CHANGE SCHEMATIC NUMBER FROM EL–1279 TO EL–1277
07–05–01 ADDED HSYNC AND VSYNC
07–09–01 ADDED N+ SUB V SIGNAL (replaces Vdd in cable path)

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

PIN ASSIGNMENTS
ANALOG BOARD OUTPUT CONNECTORS
HI RHO CCD CONTROLLER

DES'N BY: B. Alcott
ORIGIN DATE: 02–27–00
Last SN:
MODIFY DATE: 07–09–01
PATH: HI_RHO_CCD\HI_RHO_ANALCON
REV. A

DWG. NO. EL–1277
NUM. 1 OF 1